

# **Grace Hopper Conference Workshop: Nanometer Challenges and Opportunities to Microprocessor Design**

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## ***Objectives***

The workshop will review the state of art in nanometer Silicon technology, computer architectures, and circuits and discuss difficulties and potential solutions in all disciplines.

## ***Attendees***

We are targeting but not limited to students and young investigators who are looking for challenging problems to solve in modern electronics.

## ***Format of the workshop***

The workshop includes three presentations followed by Q & A. The total workshop length is 90-minutes.

## ***Abstract***

In the last three decades, the world of microprocessors has witnessed phenomenal advances - its performance increased by five orders of magnitude. What has made this happen? There is no secret that it is enabled by seemingly never-ending technology scaling, improving transistor performance to increase frequency, increasing integration capacity to realize complex architectures, and reducing energy consumed per logic operation to keep power dissipation within limit. This workshop will examine the challenges and opportunities that lie ahead over the next decade as these trends continue. How do we fabricate and process devices at a scale of a few tens of nanometers, where we get awfully close to atomic level manipulation? What new microarchitectures are needed to integrate a billion transistors on a single die? What new kinds of value will those billion transistors deliver? How do we handle power dissipation and cooling when extrapolation of current trends points toward temperatures rivaling the interior of the sun? What new tradeoffs must we make when "performance at any cost" is not an option? This workshop will review the current state of the art and discuss difficulties and potential solutions in all disciplines such as device process and technology, micro-architecture, circuits, thermals, and power delivery, to overcome these barriers for microprocessor designs beyond 90 nm CMOS technology.

## ***Background of Speakers***

**Kelin Kuhn** received the B.S. in Electrical Engineering from the University of Washington in 1980, and the M.S. and Ph.D. in Electrical Engineering from Stanford University in 1985. Dr. Kuhn joined the Intel Corporation in 1997, and since joining Intel has held a variety of technical positions on the 0.35um, 130nm, and 90nm nodes,

including (most recently) serving as the integration manager for the RF/analog derivative technology on 90nm. She is presently the device manager for digital technology on the 45nm node. Prior to joining Intel, Dr. Kuhn was a tenured faculty member in the Dept. of Elec. and Comp. Engineering at the University of Washington. Dr. Kuhn is the author of numerous technical publications on optical and electronic properties of semiconductor devices as well as author of the text Laser Engineering.

**Deborah T. Marr** is a Principle Engineer at Intel. She is currently working on a next-generation processor and manages the CPU performance team in the Desktop Product Group. On the Pentium 4 processor, she was the CPU architect responsible for Hyper-Threading Technology. Deborah has worked at Intel for over thirteen years. She first joined Intel in 1988 and made significant contributions to the Intel 386SX processor, the Pentium Pro processor, and the Pentium 4 processor. Her interests are in high-performance microarchitecture and performance analysis. Deborah received her B.S. degree in EECS from the University of California at Berkeley, and her M.S. degree in ECE from Cornell University.

**Jianping (Jane) Xu** received an MSEE and a Ph.D. in Electrical and Computer Engineering from Purdue University in 1995 and 1998, respectively. She joined Intel Corporation in 1999 as a research scientist in Emerging Platform Research and later in Circuit Research of Intel Labs in Oregon. Her research interests include high-speed Internet networking infrastructure and acceleration chips, electrical and optical interconnect system and circuits, power delivery, and acoustic device design and development. She authored and co-authored 16 technical papers, and has 29 patent applications.

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