

Automated Mapping of Coarse-Grain Pipelined Applications to FPGA Systems

Doctoral Thesis for Heidi E. Ziegler

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Abstract

Configurable systems offer a unique opportunity to define application-specific architectures. These architectures offer performance advantages, where the use of customized pipelines exploits the inherent parallelism of the application. In this research, we describe a set of program analyses and an implementation that automatically map a sequential and un-annotated C program into a pipelined implementation targeted to an FPGA with multiple external memories. This research describes an automated approach to hardware design space exploration, through a collaboration between parallelizing compiler technology and high-level synthesis tools. In previous work, we described a compiler algorithm that optimizes individual loop nests, expressed in C, to derive an efficient FPGA implementation. In this research, we describe a global optimization strategy that maps multiple loop nests to a coarse-grain pipelined FPGA implementation.

We focus on the space-time tradeoffs associated with differing amounts of parallelism, communication granularities and custom data layouts. Highly optimized designs may be too large to fit within FPGA resource constraints, so we describe heuristics for reducing area requirements while minimizing the impact on global performance. We present a design space exploration algorithm, which demonstrates the potential of this approach, for automatically deriving pipelined designs from high-level sequential specifications.

The configurability of FPGA hardware and the advent of multi-FPGA platforms leads to new decision procedures for applying existing transformations. In this research, we investigate how techniques, borrowed and adapted from existing parallelizing compiler technology, can be combined with commercial synthesis tools, to automatically derive realizable and efficient designs on multiple FPGA-based architectures. In particular, the contributions are as follows:

- **Communication Analysis and Pipelining.** We define a set of compiler analyses and transformations required to automatically design the communication for application specific pipelines for FPGA-based architectures. We determine the best communication granularity, the corresponding communication placement points within the code, and the exact data that must be communicated between pipeline stages.
- **Partition and Custom Data Layout.** Our compiler algorithm finds a coarse-grain computation and data partition, along with a custom data layout. To combat the large search space, we employ several heuristics.
- **Implementation and Evaluation.** We implement our analyses and present experimental results for a set of image-processing kernels.

With the growing number of available transistors on a single die, we anticipate the emergence of multiprocessor systems-on-a-chip and reconfigurable computing architectures with the ability to incorporate (through soft-cores) various coarse-grain computing elements such as microprocessor cores, and application specific engines (ASEs). Enabling pipelined execution, communication across computing cores, task level parallelism, and data distribution across banked memories will become increasingly important issues. Our analyses will allow the automated application mapping for these emerging infrastructures.

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Biography

Heidi Ziegler has been a doctoral student at the University of Southern California (USC), in the Department of Electrical Engineering-Systems, Computer Engineering, since 1998. Over the last five years, she has been participating in research, directed by Dr. Mary Hall, within the Computational Sciences Division at USC's Information Sciences Institute. Heidi's dissertation forms part of the work on the DEFACTO project, which demonstrated preliminary end-to-end mapping of C image-processing kernels to FPGA implementations at the DarpaTech 2002 conference in July, 2002. She has co-authored 7 papers related to this project, and last year, she published two papers from her dissertation work, one on communication analysis at the ACM/IEEE Design Automation Conference (DAC03) in June and the other on search space properties for mapping coarse-grain pipelined applications to FPGAs at the Workshop for Languages and Compilers for Parallel Computing (LCPC03) in October.

Heidi has been employed at Boeing Satellite Systems for 9 years. From Fall, 1998, until Spring, 2003, Heidi was a Boeing Full-Study Doctoral Scholar. Heidi has worked as a member of the technical staff, system engineer and project lead on both flight and ground software development for the set of NASA spacecraft, the Telemetry, Tracking and Data Relay Satellites (TDRS) HIJ, that will provide communications and data relay services into the 21st century to the Space Shuttle, Hubble telescope and other NASA spacecraft. Heidi contributed to many other phases of the TDRS program development such as spacecraft-ground interface testing, mission team, and in-orbit testing. Heidi graduated with a B.A. in French languages and literature from the University of Virginia. She received a B.S. from The University of Texas at Austin in electrical engineering and an M.S. in computer engineering from the University of Southern California.